REMARKS

The office action of January 29, 2009, has been carefully reviewed and these remarks are responsive thereto. No new subject matter has been added. Claims 1-15, 35, and 36 remain pending upon entry of the present paper. Reconsideration and allowance of the instant application are respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1-15 and 35-36 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,706,216 to Carter (hereinafter referred to as "*Carter*"). Applicants respectfully traverse.

Amended independent claim 1 recites, among other features:

> "...wherein the data processing portion is configured to extract a set of bits from the configuration bit look-up table to map a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion."

Carter fails to disclose such features. Instead, *Carter* at col. 8, line 64 – col. 10, line 68 and Figs. 7-8 describes a combinational logic section 100 that includes configurable switches 101-106, 8-bit RAMs 108 and 109 and one of eight select logics 110 and 111. Even assuming (without admitting) that combinational logic section 100 (or any of the components included therein) described in *Carter* at Fig. 8 may appropriately be analogized to the recited interconnect portion, that select lines 110-1, 110-2, and 110-3 of *Carter* may appropriately be analogized to the recited bits from the configuration bit look-up table, and that the single output of each of the one of eight select logics 110 and 111 of *Carter* may appropriately be analogized to the recited plurality of outputs, *Carter* still fails to disclose mapping a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion as recited in amended claim 1. Instead, each output of the one of eight select logics 110 and 111 in *Carter* is mapped to a unique 8-bit RAM 108 and 109. Moreover, inputs A, B, C, and D are not mapped to the outputs of one of eight select logics 110 and 111 (e.g., the alleged

outputs of the interconnect portion) in *Carter*. Instead, inputs A, B, C, and D in *Carter* merely serve as timing/select input control signals to combination logic section 100.

Thus, because *Carter* fails to disclose the above-noted features of amended claim 1, claim 1 is allowable over *Carter* for at least the foregoing reasons.

Amended independent claims 35 and 36 recite features similar to those described above with respect to claim 1. As such, claims 35 and 36 are allowable for at least substantially similar reasons.

The dependent claims are allowable for at least the same reasons as their respective base claims.

CONCLUSION

All rejections having been addressed, Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same. However, if for any reason the Examiner believes the application is not in condition for allowance or there are any questions, the examiner is requested to contact the undersigned at (202) 824-3155.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Date: March 16, 2009

By: /Ross Dannenberg/

Ross A. Dannenberg
Registration No. 49,024
1100 13th Street, N.W.
Washington, D.C. 20005-4051
Tel: (202) 824-3000
Fax: (202) 824-3001